

Amendments to the Claims

1. **(Currently Amended)** A method of adjusting equalization parameters in a receiver, including the steps of:

receiving at the receiver a data stream which has data blocks with an information section and an error correction section,

correcting bits in the data block using error correction means,

measuring a bit error rate (BER) from the number of corrected bits in the data block,

changing a predetermined equalization parameter,

measuring the bit error rate (BER) after change of the predetermined parameter,

changing the predetermined equalization parameter with an amount and in a direction so as to lower the bit error rate (BER),

continuing with measuring the bit error rate (BER) and changing the predetermined equalizing parameter until an optimum is reached; and wherein the previous bit (0 or 1) preceding a sampled bit is taken into consideration, in that the receiver threshold (th) is decreased when the previous bit is 0, and is increased when the previous bit is 1, the history of occurring bits preceding the actual sampled bit is taken into consideration in that the amount and direction of adjustment is being derived from a look-up table or a circuit forming a look-up table.

2. **(Canceled)**

3. **(Canceled)**

4. **(Original)** The method of claim 1 wherein incoming data are converted into digital form and subdivided into blocks which are processed for error correction and adjustment of equalization parameter.

5. **(Canceled)**

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Previously presented) A receiver, which has an adjustable threshold, comprising

an input (DI) for receiving analog data;

a threshold decision circuit (TH) and a clock recovery unit (CR) arranged to convert analog data received at the input into digital data;

shift register means (SR) for passing the digital data stream through the receiver to a data output (DO);

an error correction means (FEC) operative to correct the digital data and to provide a bit error rate (BER) ; and

a feedback loop having adaption means (AD) for adjusting parameters of a receiver equalizer,

characterized in that

the feedback loop includes a circuit in the kind of a look-up table which, based upon the bit error rate (BER) and tap means (TM) in the shift register means (SR), provides signals indicating the amount and direction of adjustment of the receiver threshold (th), the tap means (TM) including a flip-flop (FF) for providing the value of the previous bit preceding the actual sampled bit, the look-up table circuit increasing or decreasing the value of the receiver threshold (th) for the actual received data bit.

11. (Previously presented) A receiver, which has an adjustable threshold, comprising

an input (DI) for receiving analog data;
a threshold decision circuit (TH) and a clock recovery unit (CR) arranged to convert analog data received at the input into digital data;
shift register means (SR) for passing the digital data stream through the receiver to a data output (DO);
an error correction means (FEC) operative to correct the digital data and to provide a bit error rate (BER) ; and
a feedback loop having adaption means (AD) for adjusting parameters of a receiver equalizer,
characterized in that
the feedback loop includes a circuit in the kind of a look-up table which, based upon the bit error rate (BER) and tap means (TM) in the shift register means (SR), provides signals indicating the amount and direction of adjustment of the receiver threshold (th),
the tap means (TM) including flip-flops (FF) in series and gate circuits so as to detect the direction of signal transitions (0/1 and 1/0), a pair of conditional counters (CC1, CC2; CC3, CC4) being assigned to each signal transition (0/1 and 1/0), one conditional counter of the pair sums the number of the corrected bits of one value (1), and the other counter sums the number of the corrected bits of the other value (0), the summed numbers of the counters being supplied to each an integrator (NL 1, NL 2) which provides the adjustment value to the threshold decision circuit (TH).